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RESEARCH ARTICLE

A 5–bit CMOS attenuator with low temperature and process variations for Ka-band phased-array applications

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Abstract

A 5-bit CMOS attenuator with low temperature and process variations is presented employing the proposed optimization and compensation technique to achieve low root mean square (RMS) attenuation error and phase variation. The proposed design technique includes optimizing ratio of transistors and attenuation resistors to reduce the temperature and process variations, and utilizing a temperature and process compensation circuitry to further minimize the chip-to-chip and channel-to-channel variations. The presented attenuator is fabricated in a 55 nm CMOS process and achieves a maximum attenuation of 15.5 dB with 0.5 dB-per-step resolution. Measurement results show that the maximum RMS attenuation error is 0.6 dB and phase variation is less than ±2.2°, from −45 to 85°C and between different chips or channels within frequency range from 25 to 32 GHz. The core area is 0.32 × 0.5 mm^2 excluding pads.

KEYWORDS

attenuator, CMOS switches, precision adjustable compensation circuitry, root mean square error

1 | INTRODUCTION

Attenuators are widely used as an amplitude control and gain control block in transmitter (TX) of phased-array systems.[1–4] The performance of attenuator can be affected by process deviation and temperature variation, incurring poor attenuation error and phase variation between different chips and TX/RX channels, and hence prefers compensation for the PVT.[5–9] In addition, in conventional switched Pi/T attenuators, CMOS and BiCMOS transistor switches are adopted as variable resistors to achieve a fine resolution, which further deteriorate the RMS attenuator error and transmission phase variation over PVT.[10–13] To an optimization and compensation technique, to limit the temperature and process variations of each attenuation block, with a precision adjustable compensation circuitry employed to compensate for the attenuator error and phase variation over PVT.

In this letter, a 5-bit per-step differential attenuator with low temperature and process variations is demonstrated. Measurement results show that the maximum RMS attenuation error is 0.5 dB and phase variation is less than ±2.2°, from −45 to 85°C within frequency range from 25 to 32 GHz.

2 | REALIZATION OF THE PROPOSED TECHNIQUE

Figure 1A shows the block diagram of the proposed design, a 0.5 dB-per-step differential attenuator with a precision adjustable compensation circuitry. The control voltages VC and VC switch between zero and the compensation voltage respectively, turning OFF or turning ON the individual attenuation block.

The proposed attenuator consists of five cascade attenuation blocks with inductive compensation network.[14–16] The cascade attenuation is implemented in binary weight with least significant bit) of 0.5 dB and most significant bit) of 4 dB block for the T-type, as well as a Pi-type 8 dB attenuation.[17–20] The T-type and Pi-type attenuation blocks are composed of switching shunt/series transistors, attenuation resistors and compensation inductors, as shown in Figure 1B.

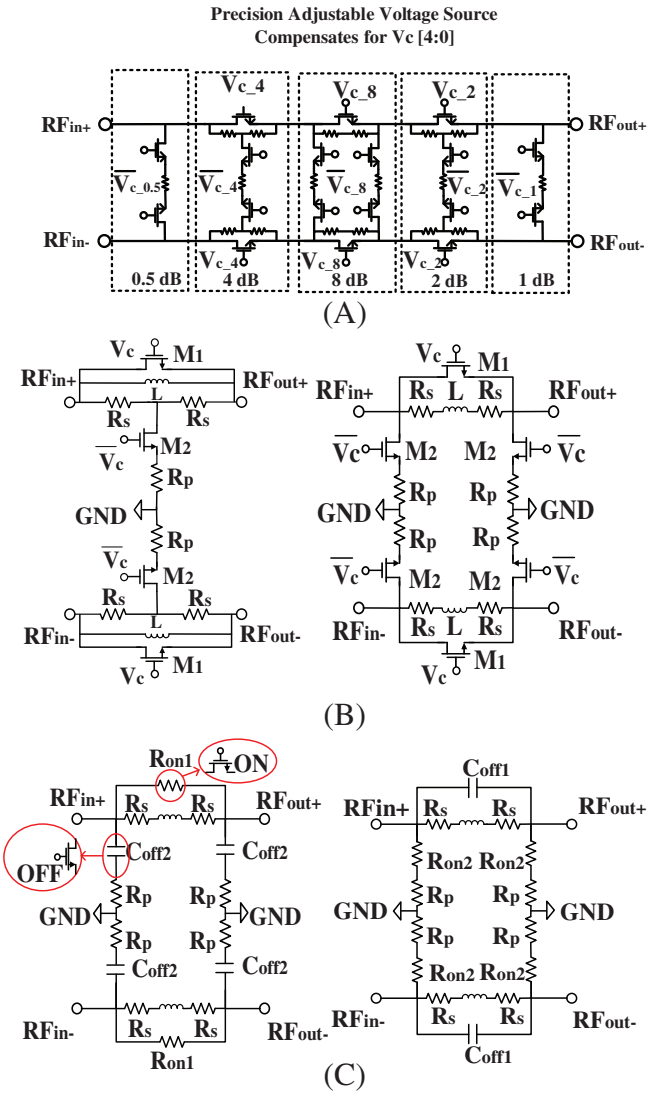

FIGURE 1 (A) Block diagram of the proposed attenuator. (B) Topologies of 5-bit differential step attenuation blocks T-type attenuation block and Pi-type attenuation block. (C) Equivalent circuits of Pi-type attenuator in the reference and attenuation states [Color figure can be viewed at wileyonlinelibrary.com]

Figure 1C shows the equivalent circuits of Pi-type attenuation block in the reference state and attenuation state. The 8 dB attenuation block is the dominant factor that affects the performance of the attenuator.[20,21] R_{on1} and R_{on2} represent the on-resistance of the series/shunt transistors M_1 and M_2. C_{off1}, C_{off2} is the off-capacitance of M_1 and M_2. The transmission phase variation is introduced by the non-zero off capacitance, and can be written as Equation (1). Z_0 is the characteristic impedance:

$$\Delta\varphi = \tan^{-1}\omega \frac{C_{off1}\left(1+\frac{R_{on2}+R_p}{Z_0^2}\right) - 2C_{off2}\left(R_{on2}+R_p\right)\left(R_{on1}+R_s\right)\left[\frac{R_{on1}R_s}{\left(R_{on1}+R_s\right)Z_0^2}+1\right]}{\left(R_{on2}+R_p\right)R_{on1}R_s} \quad (1)$$

The insertion loss is determined by R_s and R_{on1} in the reference state, as shown in Equation (2).

$$S_{21,ref} \approx \frac{1}{1+\frac{R_sR_{on1}}{2Z_0\left(R_s+R_{on1}\right)}} \quad (2)$$

And the 8 dB attenuation is realized by the series/shunt attenuation resistors R_s and R_p, and the relative attenuation can be expressed by Equation (3).

$$\Delta S_{21} = \frac{\left(R_s+R_{on1}\right)Z_0\left[2+\frac{R_s}{Z_0}+\frac{2R_s}{\left(R_{on2}+R_p\right)}+\frac{Z_0}{\left(R_{on2}+R_p\right)}\left(2+\frac{R_s}{\left(R_{on2}+R_p\right)}\right)\right]}{R_sR_{on1}+2Z_0\left(R_s+R_{on1}\right)} \quad (3)$$

To achieve good impedance matching, S_{11} of the reference state can be minimized by using large M_1 transistor. While in the attenuation state, S_{11} is determined by R_s and R_p, and can be calculated as,

$$S_{11,att} = \frac{\frac{1}{Z_0}\left[R_s\left(R_p+R_{on2}\right)-2Z_0^2\right]+\frac{Z_0R_s}{\left(R_p+R_{on2}\right)}}{\left(R_p+R_{on2}\right)\left(2+\frac{R_s}{Z_0}\right)+2\left(R_s+Z_0\right)\frac{Z_0}{\left(R_p+R_{on2}\right)^2}} \quad (4)$$

However, the switching performance of transistors, such as R_{on}, C_{off} and V_{TH}, is dependent on the process deviation and temperature variation, which further degrade the PVT performance of attenuator.[22] A method of optimization is proposed in this letter to address the above issues.

Figure 2 illustrates the optimization procedure. First, the sizes of the switching transistors are determined through temperature simulations as shown in Figure 3A. Given that the series transistor M_1 with a large W/L ratio can reduce insertion loss and reflection attributed to low R_{on1}, at the cost of phase variation degradation due to the high C_{off1}, and the shunt transistor M_2 with a small size minimizes the phase variation due to low C_{off2} at the cost of high R_{on2} which degrades the PVT performance. The optimized procedure includes:

1. The initial values of on-resistance R_{on1} and R_{on2} are set to 5 Ω (gate width of 130 μm) and 15 Ω (gate width of 50 μm), respectively. In order to ensure low insertion loss and reflection, the initial value of series resistor R_s is set to 0 Ω and the incremental step is 4 Ω. Combinations of R_{on1}/R_s and R_{on2}/R_p can be obtained.
2. A trade-off is made between attenuation and phase variation at center frequency of 28.5 GHz in this work, as shown in Figure 3B,C.
3. Note that the attenuation error of less than 1% and phase error of less than 2° are the design goals in this work, and simulations in Figure 3B,C verify that the worst case corners meet this specification. The optimum ratios of R_{on1}/R_s and R_{on2}/R_p are found to be 8 Ω/12 Ω and 8 Ω/93 Ω.

The series transistor M_1 of 90 μm (R_{on1} = 8 Ω) with R_s of 12 Ω, and the shunt transistor M_2 of 90 μm (R_{on2} = 8 Ω)

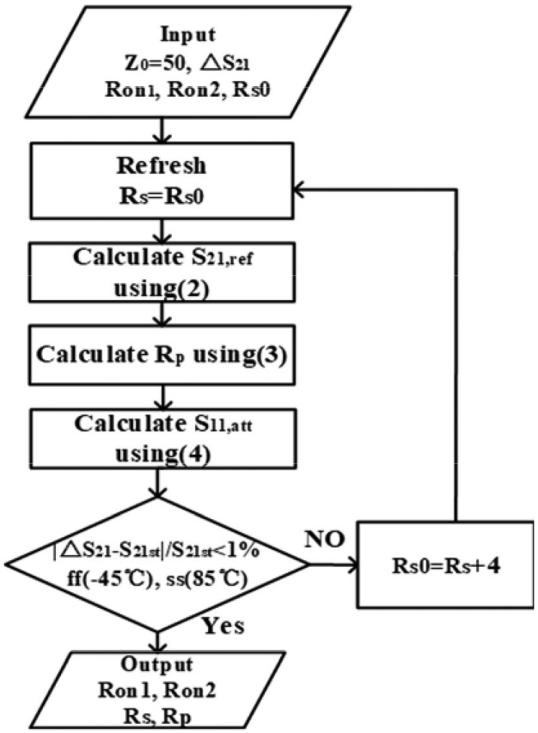

FIGURE 2 Flow chart of calculating the R_{on1}, R_{on2}, R_s and R_p

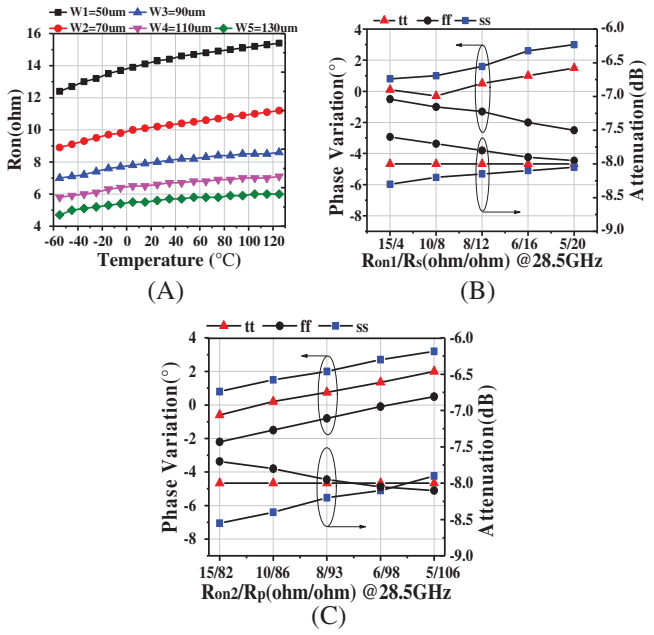

FIGURE 3 (A) Temperature simulations of R_{on} from −45 °C to 85 °C and different combinations of (B) R_{on1} and R_s (C) R_{on2} and R_p over corners [Color figure can be viewed at wileyonlinelibrary.com]

with R_p of 93 Ω for the 8 dB cell are used in this design. The parameters of the proposed attenuator are summarized in Table 1.

Based on the above optimization, the presented attenuator shows a small RMS attenuation error and phase variation by designing with the optimum ratio over PVT. In order to further improve the performance, a precision adjustable compensation circuitry that tunes the gate-to-source voltage is employed.

Equations (5) and (6) show the derivative of the on-resistance Ron with respect to temperature T, and threshold voltage V_{TH} as a function of T, respectively, where M is constant and V_{TH} (T_a) is the threshold voltage at room temperature T_a.

$$\frac{\partial R_{on}(T)}{\partial T} = \frac{\partial\left\{\left[\mu_n C_{ox} W/L (V_{GS} - V_{TH}(T))\right]^{-1}\right\}}{\partial T} \tag{5}$$

$$V_{TH}(T) = V_{TH}(T_a) - M(T - T_a) \tag{6}$$

Setting Equation (5) to be zero and solve for Equation (6), the targeted compensation voltage V_{GS} can be obtained as shown in Equation (7), where N and C are constant and determined by simulation, as used in the proposed compensation circuitry.

$$V_{GS}(T) \approx NT + C \tag{7}$$

Figure 4A shows the schematic of precision adjustable compensation circuitry, which consists of an operational amplifier, a 4-bit output DAC and BJT transistors Q_1, Q_2. The size ratio of Q_1 and Q_2 is 1/n, I_{c1} and I_{c2} are collector current of Q_1 and Q_2. So I_{c2} equals to nI_{c1}, the base–emitter voltages V_{BE} of Q_1 and Q_2 as shown in Equation (8) and (9), where I_S and V_{TH} are reverse saturation current and threshold voltage, respectively, V_{TH} equals to KT/q:

$$V_{BE1} = V_{TH} \ln\left(I_{c1}/I_S\right) \tag{8}$$

$$V_{BE2} = V_{TH} \ln\left(I_{c2}/I_S\right) \tag{9}$$

The operational amplifier is used to make voltage V_X equal to V_Y, the source voltage V_{DD} is constant voltage of 2.5 V. The base–emitter voltage difference ΔV_{BE} can be obtained as shown in Equation (10). Therefore, the proportional to absolute temperature current ΔI can be given in Equation (11), and through a 4-bit output DAC, the targeted compensation voltage V_{GS} can be obtained. The values of n and R can be determined by simulation.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_{TH} \ln(n) \tag{10}$$

$$\Delta I = \frac{\Delta V_{BE}}{R} = \frac{KT}{qR} \ln(n) \tag{11}$$

Figure 4B shows the simulated results of R_{on} with fixed V_{GS} and variable V_{GS}, respectively. The variable V_{GS} is effective on stabilizing R_{on} over PVT. Figure 4C shows the output voltages of the compensation circuitry at all 16 states from −45 to 85°C, and the output voltage increases linearly from 0.74 V at −45°C to 1.2 V at 85°C.

The simulated RMS attenuation error of the proposed attenuator with the proposed compensation circuitry and conventional circuitry over different corners is shown in Figure 4D. The RMS attenuation error of the conventional

TABLE 1 Component values for designed the proposed attenuator

Atten.	Type	R_s/R_p (Ω)	W_1 (μm)/L_1 (nm)	W_2 (μm)/L_2 (nm)	L (pH)
0.5 dB	Bridged-T	16/200	80/55	80/55	0
1 dB	Bridged-T	25/180	90/55	80/55	80
2 dB	Bridged-T	38/75	75/55	75/55	130
4 dB	Bridged-T	42/65	75/55	85/55	220
8 dB	Pi	12/93	90/55	90/55	300

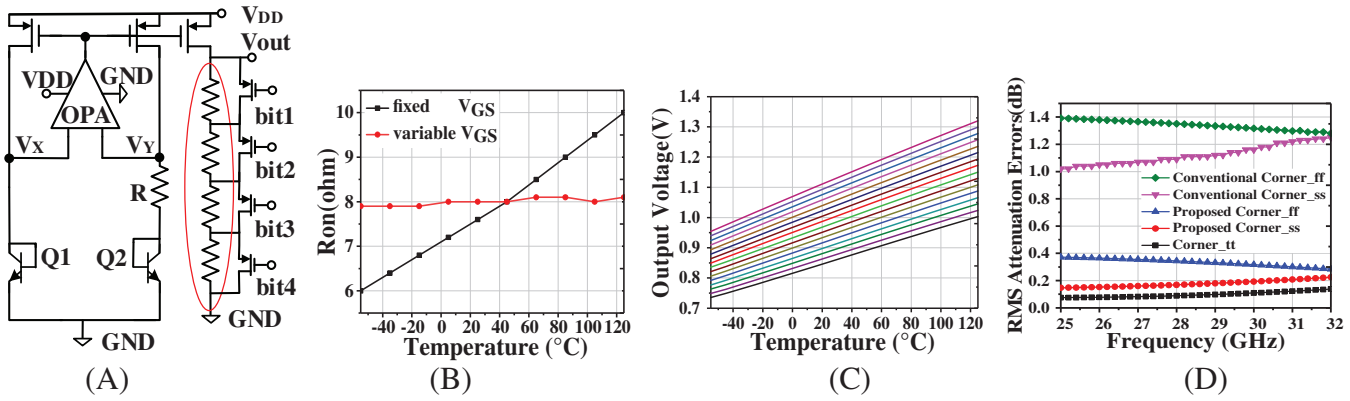

FIGURE 4 (A) Schematic of precision adjustable compensation circuitry. (B) R_{on} with stable V_{GS} and variable V_{GS} and (C) output voltage of compensation circuitry at all 16 states from −45 to 85°C. (D) Simulated root mean square (RMS) attenuation error of the proposed attenuator with conventional compensation circuitry and proposed compensation circuitry in different corners [Color figure can be viewed at wileyonlinelibrary.com]

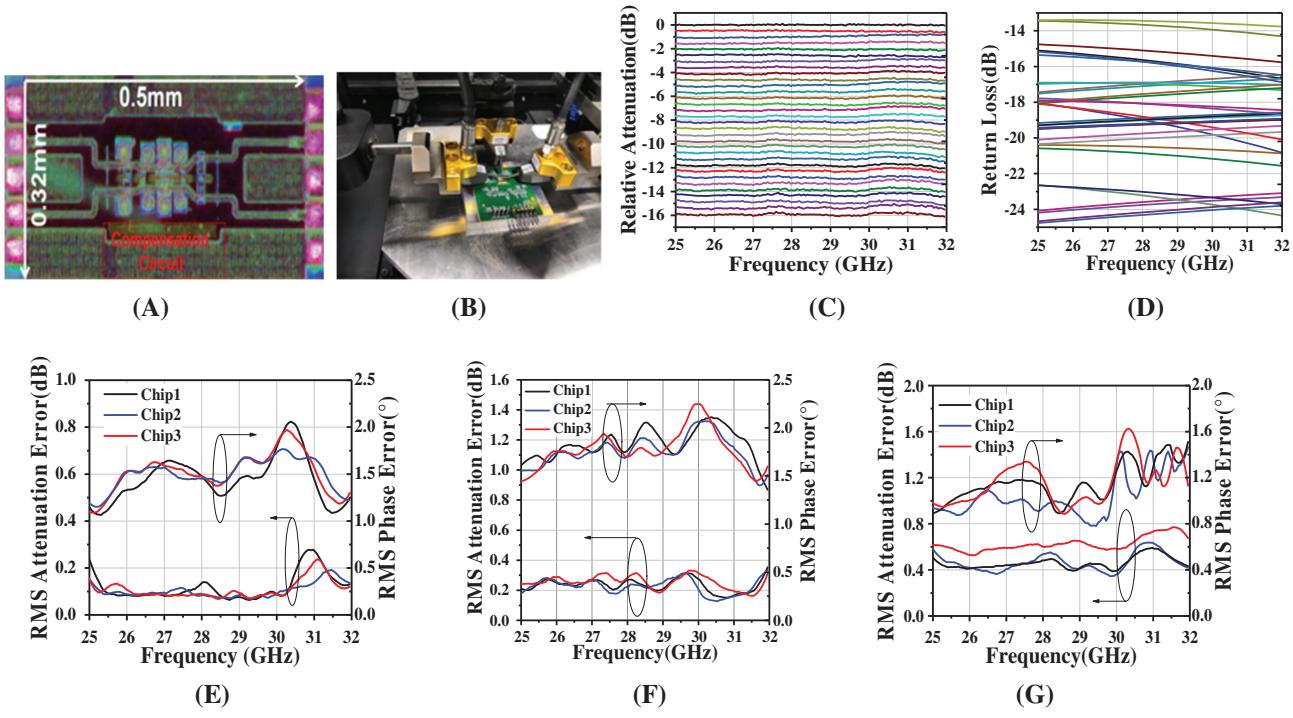

FIGURE 5 (A) Photographs of the 5-bit differential step attenuator and (B) measurement setup. (C) Relative attenuation and (D) return loss across all 32 states at 25°C. RMS attenuation error and RMS phase error of different chips across all 32 states under (E) 25°C, (F) 85°C and (G) -45°C [Color figure can be viewed at wileyonlinelibrary.com]

TABLE 2 Comparison with other attenuators

Ref.	22	16	15	20	This work
Frequency (GHz)	DC-50	25–35	8–12	23.5–30	25–32
Technology	65 nm CMOS	65 nm CMOS	0.18 μm CMOS	90 nm CMOS	55 nm CMOS
Att. range (dB)	15.5	15.5	31.5	32	15.5
Bits	5	5	6	N/A	5
LSB (dB)	0.5	0.5	0.5	0.5	0.5
IL (dB)	<6	<10	<11.3	<10	<8
RL (dB)	>12	>15	>11	>10	>13.5
RMS amp. Er. (dB)	<0.25	<0.48	<0.4	<0.42	<0.6
RMS phase. Er. (°)	<3.5	<2	<2.2	<3.1	<2.2
Die area (mm^2)	0.29	0.16	0.34	0.48	0.16
Temperature (°C)	N/A	N/A	N/A	N/A	−45, 25, 85

attenuator is 1.4 and 1.1 dB at fast corner and slow corner respectively, at 28.5 GHz, with constant bias voltage. The RMS attenuation error of the proposed attenuator is 0.3 and 0.15 dB at fast corner and slow corner, at 28.5 GHz, respectively. The proposed compensation circuitry exhibits much better performance compared with the conventional counterpart over PVT corners.

3 | MEASUREMENT RESULTS

The attenuator core area excluding pads is 0.32×0.5 mm^2, as shown in Figure 5A. The measurement setup is shown in Figure 5B. Figure 5C,D shows the measured relative attenuation and the measured input return loss across all 32 states at room temperature. The root mean square (RMS) attenuation error and RMS transmission phase error of different chips across all 32 states from −45 to 85°C, are measured as shown in Figure 5E-G. The RMS attenuation error is less than 0.6 dB and the RMS phase error is less than 2.2° over different chips. The proposed technique compensates for temperature and process variations and Table 2 compares the performance of the proposed attenuator with other state-of-the-art. This work achieves both low RMS attenuation error and phase variation over process and temperature deviations from 25 to 32 GHz.

4 | CONCLUSION

The 5-bit per-step differential attenuator utilizing the proposed technique in a 55-nm CMOS process is presented in this paper. The 5-bit per-step differential attenuator shows that the RMS phase error is less than 2.2°, and the RMS attenuation error is less than 0.6 dB from −45 to 85°C, at 25 to 32 GHz. The proposed attenuator can effectively achieve low transmission phase variation and RMS attenuation error over temperature and process variations.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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